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(54) STRAY MAGNETIC SHIELD FOR NON-VOLATIC MAGNETIC RESISTANCE MEMORY

(57) Abstract:

PROBLEM TO BE SOLVED: To obtain a non-volatile magnetic resistance memory shielding a memory from a stray magnetic field without increasing a substantial cost of a memory.

SOLUTION: A non-volatile magnetic resistance memory 10 positioned at a semiconductor substrate is shielded from a stray magnetic field by a passivation layer 18 covering partially the non-volatile magnetic resistance memory 10 or covering completely it. The passivation layer 18 comprises non- conductive ferrite materials (e.g. Mn-Zn-Ferrite, Ni-Zn-Ferrite, MnFeO, CuFeO, FeO, or NiFeO). thereby shields the non-volatic magnetic resistance memory 10 from a stray magnetic field. Non-conductive ferrite materials may be a form of a layer 18 converging a magnetic field generated internally on the non-volatile magnetic resistance memory 10 in order to decrease the requirement of power.

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CLAIMS

[Claim(s)]

[Claim 1] Are the floating MAG masking structure for non-volatile magnetic-reluctance memory, and it is positioned on :substrate. It is the passivation layer (18 60) which surrounds selectively at least non-volatile magnetic-reluctance memory (10 50); which determines an upside front face, and said non-volatile magnetic-reluctance memory (10 50). The passivation layer (18 60) concerned is floating MAG masking structure characterized by consisting of passivation layer; which covers said non-volatile magnetic-reluctance memory (10 50) from the floating MAG by it including a ferrite ingredient.

[Claim 2] Are the floating MAG masking structure for non-volatile magnetic-reluctance memory, and it is positioned on :substrate. It is the non-volatile magnetic-reluctance memory (10) which determines an upside front face. The non-volatile magnetic-reluctance memory (10) concerned Even if there are few magnetic-reluctance ingredients estranged by the layer (12) of a non-magnetic material, the 1st and the 2nd layer (11 13) are included. It is high permeability materials and is the layer (18) of a non-conductive magnetic adjuster. Non-volatile magnetic-reluctance memory of a place (10); the layer (18) concerned It is positioned near the upside front face of said non-volatile magnetic-reluctance memory (10). By it The magnetic field generated inside is converged on at least one layer the 1st of said magnetic-reluctance ingredient, and among the 2nd layer (11 13). And cover said non-volatile magnetic-reluctance memory (10) from the floating MAG. Floating MAG masking structure characterized by consisting of layer (18) layer [which is; and high permeability and surrounds selectively at least said layer which consists of a non-conductive magnetic adjuster (18) and said non-volatile magnetic-reluctance memory (10) / passivation] (18); of a place.

[Claim 3] It is the floating MAG masking structure for non-volatile magnetic-reluctance memory, and is the non-volatile magnetic-reluctance memory (50) positioned on :semi-conductor substrate (55). The non-volatile magnetic-reluctance memory (50) concerned contains the array of an individual cel (51 52) which has each cel of the magnetic-reluctance ingredient estranged by the layer of a non-magnetic material which contains the 1st layer and the 2nd layer at least. Furthermore, the non-volatile magnetic-reluctance memory (50) concerned The integrated circuit (61) which specifies and controls the individual cel (51 52) which has an input/output terminal is included. It is non-volatile magnetic-reluctance memory [of a place] (50);, and high permeability, and is the layer (60) of a non-conductive magnetic adjuster. The layer (60) concerned Even if there is little said non-volatile magnetic-reluctance memory (50), an upside front face is coated. By it Floating MAG masking structure characterized by consisting of layer (60); which converges the magnetic field generated inside on the 1st of the magnetic-reluctance ingredient in the cel according to each (51 52), and at least one layer [2nd] layer.

[Claim 4] The approach characterized by to consist of phase; which covers said non-volatile magnetic-reluctance memory from a floating magnetic field, and inactivates by [of said non-volatile magnetic-reluctance memory which has the layer of the passivation ingredient containing phase; which prepares the non-volatile magnetic-reluctance memory which is the approach of covering non-volatile magnetic-reluctance memory from a floating magnetic field, is positioned on :substrate, and determines an upside front face, and a ferrite ingredient] surrounding selectively at least.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] Generally especially this invention relates to the passivation of non-volatile magnetic-reluctance mold memory about non-volatile magnetic-reluctance memory.

[0002]

[Description of the Prior Art] The super-high density nonvolatile memory using the large-scale magnetic-reluctance (Giant Magneto-Resistive) (GMR) ingredient as a memory element accumulated using the CMOS device or the circuit has been proposed. Such memory operates using the information saved as orientation (orientation) of a magnetization vector (magnetization vectors) to a GMR memory element. Orientation of the magnetization vector is carried out by the magnetic field (H) applied. The magnetic field used in the orientation of a magnetization vector for read-out and writing is generated by the accumulation CMOS circuit. Sufficient floating magnetic field (stray magnetic field) (generated in the exterior of memory) of magnitude can become the cause which causes an error in maintenance of memory.

[0003] Floating or the magnetic field generated externally is generated from a number almost near infinity of sources. Sufficient floating magnetic field of magnitude becomes the cause of producing the magnetization vector saved in magnetic memory which carries out charge out of control. Since high density non-volatile magnetic-reluctance memory (high density non-valatile magneto-resistive memory) can do the cel very small, it is especially sensitive to a floating magnetic field. Therefore, only a magnetic field comparatively low for read-out and writing (switching or sensing of a magnetic vector) is needed. Moreover, the floating magnetic field from an adjacent cel becomes large as the distance between the adjacent cel decreases by densification.

[0004] It is designing a memory element or a memory cell which needs a switching magnetic field higher than the floating magnetic field which will encounter in the activity by the private sector or military affairs as one of the approaches which prevents the sensitivity of a floating magnetic field. This approach needs the thorough description-ization (characterization) of the floating magnetic field which will encounter in these application. Since it is not desirable in order that high internal power may need more power again, and this approach may generate a high internal magnetic field and may use it as a high power device by it, an upper limit is set as the internal power demanded in order to operate memory. The commercial scene of high density memory has an extremely intense competition. The cost gap between Millicent (milli-cents perbit) means victory or defeat per bit in a commercial scene. The addition of a production process or the advancement of the complexity of packaging makes the manufacturing cost which will determine the competitive strength of the product in a commercial scene increase.

[0005] Therefore, to offer without addition of the substantial cost of memory the non-volatile magnetic-reluctance memory covered from a floating magnetic field is desired dramatically.

[0006] It is one of the objects of this invention to offer the new and improved non-volatile magnetic-reluctance memory which has floating MAG masking structure.

[0007] It is also one of the objects of this invention without addition of the substantial cost of memory to offer the new and improved non-volatile magnetic-reluctance memory which has floating MAG masking structure.

[0008] It is also one of the objects of this invention to offer the new and improved non-volatile magnetic-reluctance memory which has the floating MAG masking structure included in a standard passivation technique.

[0009] It is also one of the objects of this invention to offer the new and improved non-volatile magnetic-reluctance memory which has the floating MAG masking structure on which the magnetic field generated inside is converged (focus).

[0010] It is also one of the objects of this invention to offer the new and improved non-volatile magnetic-reluctance memory which has the floating MAG masking structure which the magnetic field generated inside is converged and reduces the electric energy needed for operating the memory by it.

[0011] It is also one of the objects of this invention to offer the new and improved non-volatile magnetic-reluctance memory on which the magnetic field generated inside is converged.

[0012]

[Detailed explanation of a suitable example] The above-mentioned problem etc. is solved selectively at least, and the above-mentioned object etc. is realized within the non-volatile magnetic-reluctance memory which has a floating magnetic field containing the non-volatile magnetic-reluctance memory positioned on a substrate and the passivation layer which surrounds non-volatile MAG memory selectively at least. The passivation layer contains :Mn-Zn-Ferrite, nickel-Zn-Ferrite, MnFeO, CuFeO, FeO, and NiFeO as an example of a ferrite ingredient including a ferrite ingredient, in order to cover non-volatile MAG memory from a floating magnetic field.

[0013] Including the powder ferrite mixed in the layer of a passivation ingredient, various detailed application of ferrite masking offers masking to a floating magnetic field by it, covers a list on non-volatile magnetic-reluctance memory, forms the layer of a ferrite ingredient, and converges the magnetic field generated inside the same with covering the non-volatile magnetic-reluctance memory to a floating magnetic field by it. Converging the magnetic field generated inside decreases the amount of the magnetic field generated in the interior needed for switching and sensing, and, subsequently it decreases the amount of the operating power used by the non-volatile magnetic-reluctance memory.

[0014] Drawing 1 is an expanded sectional view of the example of the large-scale magnetic-reluctance GMR cel 10 which has two or more layers combined in ferromagnetism. It will be understood by this contractor that the non-volatile magnetic-reluctance memory cell 10 is only used for this description as an example, and the non-volatile magnetic-reluctance memory cell of various arbitration may be used in relation to the structure. A cel 10 has two or more magnetic layers containing the 1st magnetic layer 11 and the 2nd magnetic layer 13. Layers 11 and 13 are estranged by the 1st electric conduction spacer layer 12. Each of magnetic layers 11 and 13 may be the monolayer of a magnetic-substance ingredient, or may also be a synthetic magnetic layer instead. Furthermore, a layer 11 has the 1st thickness or thickness 23, and a layer 13 has the 2nd thickness or thickness 24 thicker than thickness 23 in a list.

[0015] In this example, layers 11 and 13 are rectangles, and along with the not a direction but longitudinal direction 27 of width of face 26, they are formed so that it may have an easy axis. It may also be made for an easy axis to meet in the width-of-face 26 direction in other gestalten of a device. Each of layers 11 and 13 met in the die-length 27 direction substantially, namely, has the magnetization vectors 21 and 22 parallel to the direction of die length 27 substantially. Here, although one set of vectors 21 and 22 exists in a cel 10, please understand that they are simultaneously illustrated in drawing 1 since the two conditions of differing are convenient. Layers 11 and 13 are combined by ferromagnetic coupling to which vectors 21 and 22 make it possible to arrange in the same direction in the condition that there is no external magnetic field. This coupling is the function of an ingredient and is the

thickness of a layer 12.

[0016] Furthermore, it is formed so that width of face 26 may become smaller than the width of face of a magnetic domain wall or a layer 11, and the migration width of face in 13 (transition width). As the result, vectors 21 and 22 cannot be made parallel with the direction of the width of face 26. Typically, as a result, width of face of less than 1.0-1.2 microns is restrained. In this example, width of face 26 is smaller than 1 micron, it is the smallness which can be manufactured by the manufacturing technology and to restrict, and die length 27 is about 5 times the width of face 26. Moreover, in this example, thickness 23 is about 3-6nm, and thickness 24 is about 4-10nm. The difference from thickness 23 and 24 influences the switching part of layers 11 and 13 as shown from now on. Vectors 21 and 22 show the two conditions of the magnetization vector in a cel 10 of differing. The condition of 1 is called in logic"0" and other conditions are logic "1." Each state vector in both the layers of layers 11 and 13 is oriented in the 1st direction, and other state vectors in both the layers of layers 11 and 13 are oriented in hard flow or the 2nd direction.

[0017] In order to write in or charge the condition of a cel 10, although switching thoroughly the direction of the magnetization vector of both the layers of layers 11 and 13 towards the reverse which met in the die-length 27 direction from one direction which met in the die-length 27 direction (the same being said of or the reverse), i.e., the condition by which it is shown by the vector 22 from the condition shown by the vector 21, switches, sufficient total magnetic field is impressed. In order to impress a total magnetic field, a longitudinal direction conductor or the WORD line 16 is formed on the front face of the dielectric layer 14 which exists on a memory cell 10, and the 2nd conductor (not shown) is connected to the edge of the opposite hand of a cel 10 in the shape of [according to individual] a row. It is used in order that association of a sense line and the WORD line 16 may also read the condition that a cel 10 is also saved (or sense). some cases -- setting -- an additional digital line (digit line) (not shown) perpendicular to the WORD line 16 -- the magnitude of a total magnetic field -- the magnetization vector -- certain -- changeover -- or it appears in causing a change enough and a certain thing is required. The magnitude of a total magnetic field is the sum of the magnetic field of the result from sense, WORD, and a digital signature current.

[0018] Drawing 2 is the graph 31 illustrating the resistance or output voltage of a cel 10 (drawing 1) to the magnetic field or total magnetic field impressed. The boss table shows the direction of a magnetic field, and its reinforcement, i.e., the reinforcement which holds or (support) carries out opposite orientation (oppose) of the magnetization vector of the cel 10. The axis of ordinate shows the output voltage of a cel 10. A curve 32 shows the magnetic field resistive characteristic of various magnetic field intensity of the one direction of the magnetization vector (for example, vector 21) through output voltage. A curve 33 shows the magnetic field resistive characteristic of the same magnetic field intensity of other directions of the magnetization vector (for example, vector 22) through output voltage. In the magnetic field to the right-hand side of 0, the output voltage of the magnetic field which holds the vector of a curve 32 and carries out opposite orientation to the vector of a curve 33 is shown, and the magnetic field to the left-hand side of 0 holds the vector of a curve 33, and curves 32 and 33 carry out opposite orientation to the vector of a curve 32. Typically, curves 32 and 33 cross on the same point of an electrical-potential-difference shaft, and have the same minimum value. For explanation, only a few is making it move perpendicularly and the curve 33 shows the difference between the curve.

[0019] The output voltage of a cel 10 is not related to 0 of an impression magnetic field almost like the direction of the magnetization vector. it is alike, and it follows, and the output voltage of the cel 10 which has the vector whose magnetic field increases from 0 to H1, and which is oriented with reverse by the total magnetic field is shown, and a curve 33 shows the electrical potential difference of the cel 10 which has the vector which boils a curve 32 in the maintenance direction by the magnetic field, and is carried out. In magnetic field intensity H1, the vector of a layer 11 converts and raises output voltage in a list. The magnetization vector of a layer 11 is maintained so that it converts, and it may be quick in other directions and may switch to them near the magnetic field intensity of H3, as total magnetic field intensity increases between H1 and H3. In the H4 neighborhood, the vector of the thicker layer 13

switches to hard flow, and resistance decreases in a value with the stronger resistance than the value of H4, and it. Similarly, the output voltage in a hard flow total magnetic field is shown between 0, and H5-H8.

[0020] The resistance is usually determined by carrying out sensing of the output voltage of a cel 10. The output voltage is a voltage drop covering the die-length direction of a cel 10 for the constant voltage impressed along the direction of the die length of a cel 10, and a magnetic field is impressed by one side. One of the approaches which determines the condition of a cel 10 is impressing the total magnetic field which is high (namely, H3), however is not the same height (namely, H4) as the change threshold of a layer 13 rather than the change threshold of a layer 11. Since the magnetic vector does not convert substantially when a total magnetic field is the direction holding the magnetic vector, i.e., the direction of the same die length 27 as a magnetization vector, resistance of a cel 10 does not change substantially. Corresponding to it, it is the output voltage and does not change substantially.

[0021] However, when a total magnetic field makes a vector hard flow, a magnetic vector converts. The vector of a layer 11 begins (the vector of a layer 13 converts slightly) to convert toward the edge of the opposite hand of a layer 11 as a magnetic field goes up. The vector of a layer 11 converts continuously, and resistance rises until the vector switches to hard flow, as a magnetic field furthermore increases. If a magnetic field goes up to be carried out, resistance will become fixed substantially and the change in the information to which it is saved will be brought about until the vector of a layer 13 also switches. And the resistance decreases with lifting of a magnetic field.

[0022] Since a cel 10 operates also as that of the premise that the value of a total magnetic field is the sum of the magnetic field produced from the current of sense, WORD, and a digital line as a result, **** from which the floating magnetic field combined with a total magnetic field may produce the substantial error in either writing or read-out actuation the same with influencing a cel 10 between the usual preservation is known. For example, a total magnetic field is higher than the change threshold of a layer 11 during read-out actuation, and when not enough to switch the magnetic vector of a layer 13, as for a floating magnetic field, ** of ** and sufficient total magnetic field which switches the information in the cel substantially can be easily impressed for H8. Furthermore, many of memory cells are dramatically small, and since it approaches dramatically and is stuffed mutually, especially in a large-scale array, the floating magnetic field of a comparatively small amount may influence a memory cell substantially. In order to ease the problem of a floating magnetic field, the passivation layer 18 is formed so that a memory cell 10 may be surrounded selectively at least. Suitably, a layer 18 is formed from the layer of a non-volatile high permeability (permeability) ingredient like a ferrite ingredient. Some ferrite ingredients which fit the object in the first half are :Mn-Zn-Ferrite, nickel-Zn-Frrite, MnFeO, CuFeO, FeO, and NiFeO, even if few. It is one. Since a layer 18 is non-conductive, when it is so electric conduction-like enough that deposition can be directly carried out on the front face of a cel 10 or a layer 18 affects actuation, the thin film 17 of dielectric materials may be used between a cel 10 and a layer 18. Since a layer 18 is formed from high permeability materials, the floating magnetic field of arbitration is covered from a cel 10. Furthermore, the magnetic field of the arbitration generated by the current supplied to the WORD line 16 is oriented toward a cel 10 top by the layer 18, or converges, and in order to attain the total magnetic field of the same amount as the smaller amount of a current is needed for read-out and/or writing by it, the WORD line 16 may be supplied.

[0023] Thus, a layer 18 performs two functions, converge [covering the cel 10 to a floating magnetic field, and] the magnetic field generated inside in a cel 10 on a list. When asking only for a masking function, a layer 18 is formed from the typical passivation ingredients (convenient dielectric materials of the arbitration which offers the good obstruction from external moisture etc.) which have a lot of mixed high permeability materials. Generally, it changes high permeability materials into a powder condition, and they may be mixed with the passivation ingredient of liquefied voice or semi- liquefied voice. And next, it is applied to the cel or array, or high permeability materials are mould pan **** to the surroundings of a cel. Moreover, sputtering of the high permeability materials is

carried out along with a passivation ingredient, or spin-on may be carried out. In other application techniques, spray coating of the powder of a ferrite ingredient may be dramatically carried out to a package on a passivation layer or the rear face of a substrate as the deposition approach of low cost.

[0024] In drawing 3 , the expanded sectional view which the array 50 of a cel similar to a cel 10 simplified is shown. Since a part of mere array 50 is convenient, it is illustrated, and it contains cels 51 and 52. Typically, two or more cels (51 for example, 52) similar to a cel 10 are formed on the common substrate 55 which has a tooth space among the cels 51 and 52 according to each etc. Next, a conductor 56 is applied to the interconnect cels 51 and 52 of the row according to individual (sense line) etc. Two or more longitudinal direction conductors or WORD lines 57 are overlapped on the memory cell relating with each column and each of memory cells.

[0025] The passivation layer 60 is continued and formed on the whole array, and the whole array and the integrated circuit (shown by 61 as a gestalt of a block) accompanying the array are thoroughly inactivated by it. Suitably, the passivation layer 60 is formed from the layer of the spin-on which used the conventional technique of arbitration, or the ferrite ingredient by which sputtering is carried out. If the whole passivation layer 60 is formed, opening 65 will be formed through the passivation layer 60, and will once enable connection to a bonding pad etc. by it. In this suitable example, the passivation layer 60 converges and orients the magnetic field (namely, magnetic field generated according to the current in the WORD line 57) generated inside not only masking and inactivation of an array but on a related cel. As mentioned above, if it asks only for the function of masking and inactivation, the passivation layer 60 will be formed from the powder condition object or the small particle of the high permeability materials mixed.

[0026] Thus, it is new and the non-volatile magnetic-reluctance memory which has the improved floating MAG masking structure was indicated. Since offering this floating MAG masking structure is included in the technique which is simple and easy and has generally already been positioned as a standard passivation technique, it does not make the cost of memory increase substantially. Suitably, it is new and the floating MAG masking structure of also accumulating the improved non-volatile magnetic-reluctance memory also converges the magnetic field generated inside the memory. Focusing of a magnetic field accompanying clearance of the floating MAG enables the magnetic field generated inside to decrease substantially, and that reduces the power of a complement to start memory. Furthermore, the focusing reduces the power consumption of a cel, decreases metal current density, and improves the dependability of a related metal. The focusing reduces the size of an actuation transistor and raises the stereo occupancy effectiveness (real estate efficiency) of a cel by it again.

[Brief Description of the Drawings]

[Drawing 1] The expanded sectional view according to this invention which a part of non-volatile magnetic-reluctance memory simplified.

[Drawing 2] Drawing which expressed with the graph the magnetic field needed for the switching condition in the non-volatile magnetic-reluctance memory of drawing 1 .

[Drawing 3] The sectional view which the high density non-volatile magnetic-reluctance memory according to this invention simplified.

[Description of Notations]

10 50 Non-volatile magnetic-reluctance memory cell

11 13 Magnetic-reluctance ingredient layer

12 Non-magnetic Material Layer

14 Dielectric Layer

16 WORD Line

17 Thin Film of Dielectric Materials

18 Passivation Layer

21 22 Vector

23 24 Thickness

26 Width of Face

27 Die Length

31 Graph

32 33 Curve

51 52 Cel

55 Substrate

56 Conductor

57 WORD Line

60 Passivation Layer

61 Integrated Circuit

65 Opening

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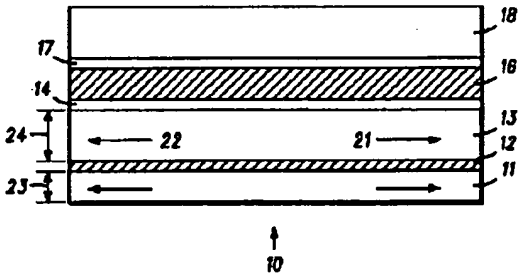
最終頁に続く

(54)【発明の名称】　不揮発性磁気抵抗メモリのための浮遊磁気遮へい

(57)【要約】

【課題】　メモリの実質的なコストの付加なしに、浮遊磁場から遮へいする不揮発性磁気抵抗メモリを提供する。

【解決手段】　半導体基板上に位置づけられる不揮発性磁気抵抗メモリ（１０）が、不揮発性磁気抵抗メモリ（１０）を部分的に、または完全に囲むパッシベーション層（１８）によって浮遊磁場から遮へいせられる。そのパッシベーション層（１８）は、非導電性フェライト材料（例えば、Mn-Zn-Ferrite,Ni-Zn-Ferrte,MnFeO,CuFeO,FeOまたはNiFeO）を含み、それによって、不揮発性磁気抵抗メモリ（１０）を浮遊磁場から遮へいする。非導電性フェライト材料はまた、電力要求を減少させるために、不揮発性磁気抵抗メモリ（１０）上に内部で発生する磁場を集束させる層（１８）の形態でもよい。



【特許請求の範囲】

【請求項１】　不揮発性磁気抵抗メモリのための浮遊磁気遮へい構造であって：基板上に位置づけられ、上側表面を決定する不揮発性磁気抵抗メモリ（１０、５０）；および前記不揮発性磁気抵抗メモリ（１０、５０）を少なくとも部分的に囲むパッシベーション層（１８、６０）であって、当該パッシベーション層（１８、６０）は、フェライト材料を含み、それによって、前記不揮発性磁気抵抗メモリ（１０、５０）を浮遊磁気から遮へいする、ところのパッシベーション層；から構成されることを特徴とする浮遊磁気遮へい構造。

【請求項２】　不揮発性磁気抵抗メモリのための浮遊磁気遮へい構造であって：基板上に位置づけられ、上側表面を決定する不揮発性磁気抵抗メモリ（１０）であって、当該不揮発性磁気抵抗メモリ（１０）は、非磁性材料の層（１２）によって離間せられる磁気抵抗材料の少なくとも第１および第２層（１１、１３）を含む、ところの不揮発性磁気抵抗メモリ（１０）；高透磁率材料であり、かつ非導電性磁気材料の層（１８）であって、当該層（１８）は、前記不揮発性磁気抵抗メモリ（１０）の上側表面の近くに位置づけられ、それによって、内部で発生する磁場を前記磁気抵抗材料の第１および第２層（１１、１３）のうち少なくとも１つの層に集束し、かつ浮遊磁気から前記不揮発性磁気抵抗メモリ（１０）を遮へいする、ところの層（１８）；および高透磁率であり、かつ非導電性磁気材料（１８）および前記不揮発性磁気抵抗メモリ（１０）から成る前記層を少なくとも部分的に囲むパッシベーション層（１８）；から構成されることを特徴とする浮遊磁気遮へい構造。

【請求項３】　不揮発性磁気抵抗メモリのための浮遊磁気遮へい構造であって：半導体基板（５５）上に位置づけられる不揮発性磁気抵抗メモリ（５０）であって、当該不揮発性磁気抵抗メモリ（５０）は、非磁性材料の層によって離間せられる磁気抵抗材料の少なくとも第１層および第２層を含む各セルを有する個別セル（５１、５２）のアレイを含み、さらに、当該不揮発性磁気抵抗メモリ（５０）は、入力／出力端子を有する個別セル（５１、５２）を指定し制御する集積回路（６１）を含む、ところの不揮発性磁気抵抗メモリ（５０）；および高透磁率であり、かつ非導電性磁気材料の層（６０）であって、当該層（６０）は、前記不揮発性磁気抵抗メモリ（５０）の少なくとも上側表面をコーティングし、それによって、内部で発生する磁場を、各個別のセル（５１、５２）内の磁気抵抗材料の第１および第２層の少なくとも１つの層上に集束させる、ところの層（６０）；から構成されることを特徴とする浮遊磁気遮へい構造。

【請求項４】　浮遊磁場から不揮発性磁気抵抗メモリを遮へいする方法であって：基板上に位置づけられ、上側表面を決定する不揮発性磁気抵抗メモリを準備する段階；およびフェライト材料を含むパッシベーション材料の層を有する前記不揮発性磁気抵抗メモリの少なくとも部分的に囲むことによって、前記不揮発性磁気抵抗メモリを、浮遊磁場から、遮へいし、かつ不活性化する段階；から構成されることを特徴とする方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は一般に不揮発性磁気抵抗メモリに関し、特に不揮発性磁気抵抗型メモリのパッシベーションに関する。

【０００２】

【従来の技術および発明が解決しようとする課題】CMOSデバイスまたは回路を用いて集積したメモリ要素としての大規模磁気抵抗（Giant Magneto-Resistive）（GMR）材料を利用した、超高密度不揮発性メモリが提案されてきた。これらのメモリは、GMRメモリ要素に磁化ベクトル（magnetization vectors）の配向（orientation）として保存される情報によって動作する。その磁化ベクトルは、適用される磁場（H）によって、配向される。磁化ベクトルの配向を読出しおよび書込みのために使用されるその磁場は、集積CMOS回路によって生成される。十分な大きさの浮遊磁場（stray magnetic field）（メモリの外部で生成される）が、メモリの保持にエラーを引き起こす原因になり得る。

【０００３】浮遊または外部的に生成される磁場は、ほとんど無限に近い数の源から発生する。十分な大きさの浮遊磁場は、制御不能なチャージをするような、磁気メモリに保存される磁化ベクトルを生じさせる原因になる。高密度不揮発性磁気抵抗メモリ（high density non-valatile magneto-resistive memory）は、そのセルが非常に小さくできるので、浮遊磁場に、特に敏感である。したがって、読出しおよび書込み（磁気ベクトルのスイッチングまたはセンシング）のために比較的低い磁場しか必要としない。また、高密度化によってその隣り合うセル間の距離が減小するに従い、隣り合うセルからの浮遊磁場が大きくなる。

【０００４】浮遊磁場の敏感性を防止する方法の一つとしては、民間または軍事での使用において遭遇するであろう浮遊磁場よりも高いスイッチング磁場を必要とするようなメモリ要素またはメモリセルを設計することである。この方法は、これらの適用において遭遇するであろう浮遊磁場の徹底的な特徴化（characterization）を必要とする。この方法は、また、高い内部電力がより多くの電力を必要とし、高い内部磁場を生成し、それによって高電力デバイスにするため望ましくないので、メモリを動作させるために要求される内部電力に、上限を設定する。高密度メモリの市場は極端に競争が激しい。ビットあたりミリセント（milli-cents perbit）の間でのコスト格差が、市場では勝敗を意味する。製造工程の追加またはパッケージングの複雑さの高度化が、市場における製品の競争力を決定するであろう製造コストを増加さ

せる。

【０００５】したがって、メモリの実質的なコストの付加なしに、浮遊磁場から遮へいする不揮発性磁気抵抗メモリを提供することが、非常に望まれる。

【０００６】浮遊磁気遮へい構造を有する新規であり、改善された不揮発性磁気抵抗メモリを提供することが、本発明の目的の１つである。

【０００７】メモリの実質的なコストの付加なしに、浮遊磁気遮へい構造を有する新規であり、改善された不揮発性磁気抵抗メモリを提供することも、本発明の目的の１つである。

【０００８】標準的なパッシベーション技術に組み込まれる、浮遊磁気遮へい構造を有する新規であり、改善された不揮発性磁気抵抗メモリを提供することも、本発明の目的の１つである。

【０００９】内部で発生する磁場を集束（focus）させる、浮遊磁気遮へい構造を有する新規であり、改善された不揮発性磁気抵抗メモリを提供することも、本発明の目的の１つである。

【００１０】内部で発生する磁場を集束させ、それによって、そのメモリを動作させるのに必要とされる電力量を削減する、浮遊磁気遮へい構造を有する新規であり、改善された不揮発性磁気抵抗メモリを提供することも、本発明の目的の１つである。

【００１１】内部で発生する磁場を集束させる、新規であり、改善された不揮発性磁気抵抗メモリを提供することも、本発明の目的の１つである。

【００１２】

【好適実施例の詳細な説明】上記問題等は少なくとも部分的に解決され、上記の目的等は、基板上に、および少なくとも部分的に不揮発性磁気メモリを囲むパッシベーション層上に、位置づけられる不揮発性磁気抵抗メモリを含む浮遊磁場を有する不揮発性磁気抵抗メモリ内で実現される。そのパッシベーション層は、浮遊磁場から不揮発性磁気メモリを遮へいするためにフェライト材料を含み、フェライト材料の例としては：Mn-Zn-Ferrite,Ni-Zn-Ferrite,MnFeO,CuFeO,FeOおよびNiFeOを含む。

【００１３】フェライト遮へいの様々な詳細な適用が、パッシベーション材料の層内に混合した粉状フェライトを含み、それによって浮遊磁場に対して遮へいを提供し、並びに不揮発性磁気抵抗メモリの上に亘って、フェライト材料の層を形成し、それによって、浮遊磁場に対する不揮発性磁気抵抗メモリを遮へいすることと同様に、内部で発生する磁場を集束させる。内部で発生する磁場を集束させることは、スイッチングおよびセンシングに必要とされる内部で発生する磁場の量を減少させ、次いで、その不揮発性磁気抵抗メモリによって使用される動作電力の量を減少させる。

【００１４】図１は、強磁性的に結合される複数の層を有する大規模磁気抵抗GMRセル１０の例の拡大断面図である。不揮発性磁気抵抗メモリセル１０は、単に例として本明細書に使用され、様々な任意の不揮発性磁気抵抗メモリセルがその構造と関連して使用され得ることが、当業者には理解されるであろう。セル１０が、第１磁性体層１１および第２磁性体層１３を含む複数の磁性体層を有する。層１１、１３は、第１導電スペーサ層１２によって離間せられる。磁性体層１１、１３のそれぞれは、磁性体材料の単一層であり得る、または、替りに合成磁性体層でもあり得る。さらに、層１１は、第１の厚さまたは厚さ２３を有し、並びに層１３は、厚さ２３よりの厚い第２の厚さまたは厚さ２４を有する。

【００１５】この実施例においては、層１１、１３は、長方形であり、幅２６の方向ではなく、長手方向２７に沿って、磁化容易軸を有するように、形成される。デバイスの他の形態においては、磁化容易軸は、幅２６の方向に沿うようにもし得る。層１１、１３のそれぞれは、実質的に長さ２７の方向に沿った、すなわち、実質的に長さ２７の方向に平行である、磁化ベクトル２１、２２を有する。ここで、ベクトル２１、２２の１セットがセル１０に存在するが、２つの異なる状態が、便利のために、図１において同時に図示されていることを理解されたい。ベクトル２１、２２が、外部磁場の無い状態において、同一方向に並べることを可能にする強磁性カップリングによって、層１１、１３が結合せられる。このカップリングは、材料の機能であり、層１２の厚さである。

【００１６】さらに、幅２６が、磁壁の幅または層１１、１３内の移動幅（transition width）よりも小さくなるように、形成される。その結果として、ベクトル２１、２２は、その幅２６の方向と平行にすることができない。典型的に、1.0～1.2ミクロン未満の幅が、結果的には、拘束になる。この実施例においては、幅２６は、1ミクロンより小さく、製造技術によって製造可能なかぎりの小ささであり、長さ２７は幅２６の約５倍である。また、この実施例においては、厚さ２３は、約3～6nmであり、厚さ２４は約4～10nmである。これから示すとおり、厚さ２３と２４との違いは、層１１、１３のスイッチング部分に影響する。ベクトル２１、２２は、セル１０内の磁化ベクトルの２つの異なる状態を示している。１の状態は、論理”０”を呼ばれ、他の状態は、論理”１”である。層１１、１３の両層における各状態ベクトルは第１方向に方向付けられ、層１１、１３の両層における他の状態ベクトルは、逆方向または第２方向に方向付けられる。

【００１７】セル１０の状態を書込むまたはチャージするために、長さ２７の方向に沿った１方向から長さ２７の方向に沿った逆の方向へ層１１、１３の両層の磁化ベクトルの方向を完全に切り換えるのに、すなわち、ベクトル２１によって示されている状態からベクトル２２によって示される状態へ（またはその逆も同様）の切り換

えるのに、十分なトータル磁場が、印加される。トータル磁場を印加するために、横方向導電体またはワードライン１６が、メモリセル１０の上に存在する誘電体層１４の表面上に形成され、第２導電体（図示せず）が、個別の横列状にセル１０の反対側の端に接続される。センスラインおよびワードライン１６の結合もまた、セル１０も保存される状態を読み出す（またはセンス）ために使用される。いくつかの場合においては、ワードライン１６に垂直方向である付加的なデジタルライン（digit line）（図示せず）が、トータル磁場の大きさがその磁化ベクトルが確実に転換かまたは切換えを引き起こすのに十分であることが要求される。トータル磁場の大きさは、センス、ワードおよびデジタルサイン電流からの結果の磁場の和である。

【００１８】図２は、印加される磁場またはトータル磁場に対するセル１０（図１）の抵抗値または出力電圧を図示したグラフ３１である。その横座表は、磁場方向およびその強度、すなわち、そのセル１０の磁化ベクトルを保持（support）するまたは逆向（oppose）する強度、を示す。その縦軸は、セル１０の出力電圧を示す。曲線３２が、出力電圧を介した、磁化ベクトル（例えばベクトル２１）の１方向の様々な磁場強度の、磁場抵抗特性を示す。曲線３３が、出力電圧を介した、磁化ベクトル（例えばベクトル２２）の他の方向の同様な磁場強度の、磁場抵抗特性を示す。０の右側への磁場では、曲線３２、３３は、曲線３２のベクトルを保持し、かつ曲線３３のベクトルに逆向する磁場の出力電圧を示し、０の左側への磁場は、曲線３３のベクトルを保持し、かつ曲線３２のベクトルに逆向する。典型的に、曲線３２、３３は、電圧軸の同一ポイントで交差し、同一の最小値を有する。説明のために、曲線３３は、少しだけ垂直方向に移動させており、その曲線間の相違を示している。

【００１９】印加磁場の０においては、セル１０の出力電圧は、その磁化ベクトルの方向とほぼ同様に関係ない。０からＨ１まで磁場が増加するに従って、曲線３３は、トータル磁場によって逆に方向付けられるベクトルを有するセル１０の出力電圧を示し、曲線３２はその磁場によって保持方向ににされるベクトルを有するセル１０の電圧を示す。磁場強度Ｈ１において、層１１のベクトルは、出力電圧を転向し、並びに上昇させる。トータル磁場強度がＨ１とＨ３との間で増加するにつれ、層１１の磁化ベクトルが、Ｈ３の磁場強度付近で他の方向に転向、すばやく切り換わるように持続される。Ｈ４付近では、より厚い層１３のベクトルが、逆方向に切り換わり、ならびにその抵抗はＨ４の値およびそれより大きい値では、抵抗値が減少する。同様に、逆方向トータル磁場での出力電圧が、０とＨ５～Ｈ８との間に示される。

【００２０】その抵抗値は、通常、セル１０の出力電圧をセンシングすることによって決定される。その出力電圧は、セル１０の長さの方向に沿って印加される定電圧をセル１０の長さ方向に亘っての電圧降下であり、一方で磁場が印加される。セル１０の状態を決定する方法の１つは、層１１の切換えしきい値よりも高く（すなわちＨ３）であって、しかし層１３の切換えしきい値と同じ高さ（すなわちＨ４）ではないトータル磁場を印加することである。トータル磁場が、その磁気ベクトルを保持する方向、すなわち磁化ベクトルと同じ長さ２７の方向である場合、その磁気ベクトルは、実質的に転向しないので、セル１０の抵抗は実質的に変化しない。それに対応して、その出力電圧のまた実質的に変化しない。

【００２１】しかし、トータル磁場がベクトルを逆方向にする場合、磁気ベクトルは転向する。磁場が上昇するにつれ、層１１のベクトルは、層１１の反対側の端に向かって転向し始める（層１３のベクトルはわずかに転向する）。さらに磁場が増加するにつれ、層１１のベクトルは、転向し続け、抵抗値は、そのベクトルが逆方向に切り換わるまで上昇する。されに磁場が上昇すると、層１３のベクトルも切り換わるまで、抵抗値は実質的に一定になり、それが保存されている情報における変化をもたらす。それから、その抵抗値は磁場の上昇とともに減小する。

【００２２】トータル磁場の値が、センス、ワードおよびデジタルラインの電流から結果として生ずる磁場の和であるという前提のもとセル１０が動作するので、トータル磁場と結合する浮遊磁場が、通常の保存の間にセル１０に影響するのと同様に、書込みまたは読出し動作のいずれかにおける実質的なエラーを生じ得るこたがわかる。例えば、読出し動作の間、トータル磁場が層１１の切換えしきい値よりも高く、かつ層１３の磁気ベクトルを切換えるには十分でない場合、浮遊磁場は、Ｈ８をじのぎ、実質的にそのセル内の情報を切換えるような、十分なトータル磁場を簡単に印加することができる。さらに、メモリセルの多くが非常に小さく、互いに非常に接近して詰め込まれているので、特に大規模アレイにおいては、比較的小さい量の浮遊磁場がメモリセルに実質的に影響し得る。浮遊磁場の問題を緩和するために、パッシベーション層１８が、メモリセル１０を少なくとも部分的に囲むように形成される。好適には、層１８は、フェライト材料のような不揮発性高透磁率（permeability）材料の層から形成される。前期目的に適するいくつかのフェライト材料は少なくとも：Mn-Zn-Ferrite,Ni-Zn-Frrite,MnFeO,CuFeO,FeOおよびNiFeO　のうちの１つである。層１８は非導電性であるので、セル１０の表面上に直接にデポジションすることができ、若しくは層１８が動作に影響を与えるほど十分に導電的である場合、誘電体材料の薄膜１７がセル１０と層１８との間に使用され得る。層１８が高透磁率材料から形成されるので、任意の浮遊磁場は、セル１０から遮へいされる。さらに、ワードライン１６に供給される電流によって生成される任意の磁場が、層１８によってセル１０上に向かっ

て方向付けられて、若しくは集束し、それによって、電流のより少ない量が、読出しおよび／または書込みに必要とされるのと同じ量のトータル磁場を達成するために、ワードライン１６に供給され得る。

【００２３】このように、層１８は、浮遊磁場に対するセル１０を遮へいすること、並びにセル１０内に内部で発生する磁場を集束することの２つの機能を実行する。遮へい機能のみが所望される場合、層１８は、混合された多量の高透磁率材料を有する典型的なパッシベーション材料（外部の湿気からの良い障壁を提供する任意の便利な誘電体材料など）から形成される。一般に、高透磁率材料は、粉末状態にされ、液状態または準液状態のパッシベーション材料と混合せられ得る。そして次に、高透磁率材料は、そのセルまたはアレイに適用され、若しくはセルの周りにモールドされる。また、高透磁率材料は、パッシベーション材料に沿ってスパッタリングされるか、若しくはスピンオンされ得る。他の適用技術においては、非常に低コストのデポジション方法として、フェライト材料のパウダが、パッシベーション層上に、または基板の裏面上に、またはパッケージに、スプレイコーティングされ得る。

【００２４】図３において、セル１０に類似するセルのアレイ５０の簡単化した拡大断面図が示されている。アレイ５０のほんの一部分が、便利のために図示され、セル５１、５２を含む。代表的には、セル１０に類似した複数のセル（例えば５１、５２）が、各個別のセル５１、５２などの間にスペースを有する共通の基板５５上に形成される。次に、導電体５６が、個別の横列（センスライン）の相互接続セル５１、５２などに適用される。複数の横方向導電体またはワードライン５７が、メモリセルの各縦列とその１つ１つが関係して、そのメモリセルの上に重畳する。

【００２５】パッシベーション層６０が、アレイ全体の上に亘って形成され、それによって、完全に、そのアレイ全体およびそのアレイに伴う集積回路（６１でブロックの形態として示される）を不活性化する。好適には、パッシベーション層６０は、任意の従来技術を使用したスピンオンまたはスパッタリングされるフェライト材料の層から形成される。一旦、パッシベーション層６０の全体が形成されると、開口６５が、パッシベーション層６０を介して形成され、それによってボンディングパッドなどへの接続を可能にする。この好適実施例においては、パッシベーション層６０は、アレイの遮へいおよび不活性化のみならず、関連するセル上に、内部で発生する磁場（すなわち、ワードライン５７内の電流によって発生する磁場）を集束し、方向付ける。前記の様に、遮へいおよび不活性化の機能のみが所望されているならば、パッシベーション層６０は、混合せられる高透磁率材料の粉状態物または小さいパーティクルから形成される。

【００２６】このように、新規であり、改善された浮遊磁気遮へい構造を有する不揮発性磁気抵抗メモリが、開示された。この浮遊磁気遮へい構造は、提供するのが、単純かつ簡単であり、一般に、例えば標準的なパッシベーション技術として既に位置づけられている手法に組み込まれるので、実質的にメモリのコストを増加させない。好適には、新規であり、改善された不揮発性磁気抵抗メモリもための浮遊磁気遮へい構造もまた、そのメモリの内部で発生する磁場を集束する。浮遊磁気の除去に伴う、磁場の集束は、内部で発生する磁場が、実質的に減少することを可能にし、そのことは、メモリを起動させるのに必要な量の電力を削減する。さらに、その集束は、セルの消費電力を削減し、金属電流密度を減少させ、関連する金属の信頼性を改善する。その集束はまた、駆動トランジスタのサイズを削減し、それによって、セルの実体占有効率（real estate efficiency）を向上させる。

【図面の簡単な説明】

【図１】本発明に従った、不揮発性磁気抵抗メモリの一部分の簡単化した拡大断面図。

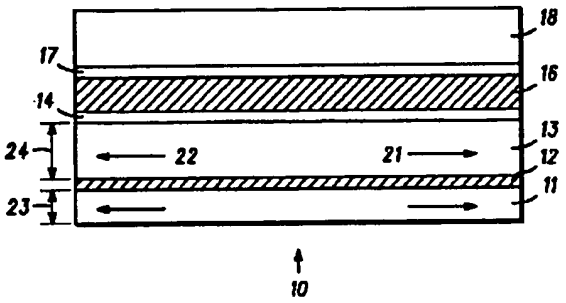
【図２】図１の不揮発性磁気抵抗メモリにおけるスイッチング状態に必要とされる磁場をグラフに表した図。

【図３】本発明に従った、高密度不揮発性磁気抵抗メモリの簡単化した断面図。

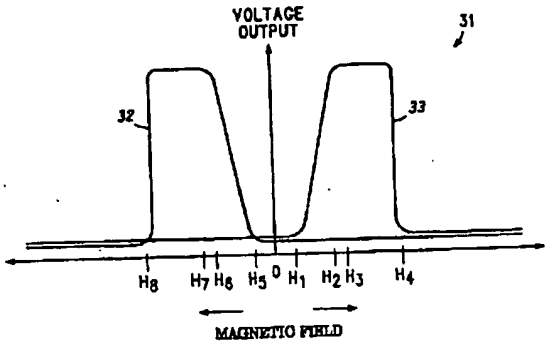
【符号の説明】

１０、５０　不揮発性磁気抵抗メモリセル
１１、１３　磁気抵抗材料層
１２　非磁性材料層
１４　誘電体層
１６　ワードライン
１７　誘電体材料の薄膜
１８　パッシベーション層
２１、２２　ベクトル
２３、２４　厚さ
２６　幅
２７　長さ
３１　グラフ
３２、３３　曲線
５１、５２　セル
５５　基板
５６　導電体
５７　ワードライン
６０　パッシベーション層
６１　集積回路
６５　開口

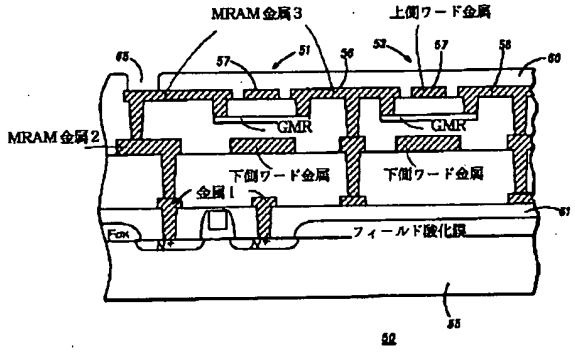
【図１】



【図２】



【図３】



フロントページの続き

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【外国語明細書】

STRAY MAGNETIC SHIELDING FOR A NON-VOLATILE MRAM

Field of the Invention

The present invention pertains to non volatile magneto-resistive memories and more specifically to passivation of non-volatile magneto-resistive memories.

Background of the Invention

Very high density non-volatile memories utilizing Giant Magneto-Resistive (GMR) materials as the memory element integrated with CMOS devices or circuits have been proposed. These memories operate by storing information as the orientation of the magnetization vectors in the GMR memory elements. The magnetization vectors are oriented by means of applied magnetic (H) fields. The magnetic fields used to read and write the orientation of the magnetization vectors are generated by the integrated CMOS circuitry. Stray magnetic fields, generated external to the memory, having sufficient magnitude could cause errors in memory retention.

Stray or externally generated magnetic fields can come from an almost infinite number of sources. Stray magnetic fields having sufficient magnitude may cause the magnetization vectors stored in a magnetic memory to change uncontrollably. High density non-volatile magneto-resistive memories are especially sensitive to stray fields because the cells are becoming very small and, hence, require relatively low fields for reading and writing (switching or sensing the magnetic vectors). Also, stray fields from neighboring cells become larger as the distance between

neighboring cells decreases at high densities.

One method of avoiding sensitivity to stray magnetic fields is t o design the memory elements or cells such that they require higher swi tching fields than the stray fields they would encounter in commercial or military use. This method requires an exhaustive characterization of t he stray fields encountered in these applications. This method also set s higher limits of internal power requirements to operate the memory, si nce higher internal fields requires more power to generate the higher in ternal fields, making them high power devices and, therefore, less desi rable. The market for high density memories is extremely competitive. C ost differentials between suppliers of milli-cents per bit can mean succ ess or failure in the market place. The addition of manufacturing steps or increased packaging complexity adds cost to the product which could determine the competitiveness of the product in the market place.

Accordingly it is highly desirable to provide a non-volatile mag neto-resistive memory which is shielded from stray magnetic fields witho ut adding substantial cost to the memory.

It is a purpose of the present invention to provide a new and im proved non-volatile magneto-resistive memory with stray magnetic shieldi ng.

It is another purpose of the present invention to provide a new and improved non-volatile magneto-resistive memory with stray magnetic s hielding which does not add substantially to the cost of the memory.

It is still another purpose of the present invention to provide a new and improved non-volatile magneto-resistive memory with stray magn etic shielding which is incorporated into the standard passivation techn ique.

It is a further purpose of the present invention to provide a ne w and improved non-volatile magneto-resistive memory with stray magnetic

shielding which also focuses the internally generated magnetic fields.

It is a still further purpose of the present invention to provide a new and improved non-volatile magneto-resistive memory with stray magnetic shielding which also focuses the internally generated magnetic fields so as to reduce the amount of power required to operate the memory.

It is a still further purpose of the present invention to provide a new and improved non-volatile magneto-resistive memory with focusing of the internally generated magnetic field.

Summary of the Invention

The above problems and others are at least partially solved and the above purposes and others are realized in a non-volatile magneto resistive memory with stray magnetic shielding including a non-volatile magneto-resistive memory positioned on a substrate and a passivation layer at least partially surrounding the non-volatile magneto-resistive memory. The passivation layer includes ferrite materials for shielding the non-volatile magneto-resistive memory from stray magnetic fields. examples of the ferrite material including: Mn-Zn-Ferrite. Ni-Zn-Ferrite. MoFeO. CuFeO, FeO, and NiFeO.

Various specific applications of the ferrite shielding include intermixing powdered ferrite in a layer of passivation material to provide shielding against stray magnetic fields and forming a layer of ferrite material over the non-volatile magneto-resistive memory to focus internally generated magnetic fields as well as shielding the non-volatile magneto-resistive memory against stray magnetic fields. Focusing the internally generated magnetic fields reduces the amount of internally generated magnetic field required for switching and sensing, which in turn reduces the amount of operating power used by the non-volatile magneto-resis

tive memory.

Brief Description of the Drawings

Referring to the drawings:

FIG. 1 is a simplified and enlarged cross-sectional view of a portion of a non-volatile magneto-resistive memory in accordance with the present invention;

FIG. 2 is a graphical representation of magnetic fields required for switching states in the non-volatile magneto-resistive memory of FIG. 1; and

FIG. 3 is a simplified cross-sectional view of a high density non-volatile magneto-resistive memory in accordance with the present invention.

Description of the Preferred Embodiments

Turning now to the drawings, FIG. 1 is an enlarged cross-sectional view of an example of a giant magnetoresistive GMR cell 10 having multiple layers that are ferromagnetically coupled. Non-volatile magneto-resistive memory cell 10 is used in this explanation only for example and it will be understood by those skilled in the art that any of a variety of non-volatile magneto-resistive memory cells can be used in conjunction with the present structure. Cell 10 has a plurality of magnetic layers including a first magnetic layer 11 and a second magnetic layer 13. Layers 11 and 13 are separated by a first conductive spacer layer 12. Magnetic layers 11 and 13 each can be single layers of magnetic materials or, alternately, can be a composite magnetic layer. Additionally, layer 11 has a first thickness or thickness 23 and layer 13 has a second thickness

r thickness 24 that is greater than thickness 23.

In this example, layers 11 and 13 are rectangular and are formed with th e easy axis of magnetization along a length 27 and not along a width 26.

In other types of devices, the easy axis can be along width 26. Layer s 11 and 13 each have magnetization vectors 21 and 22 that are substanti ally along length 27, that is, substantially parallel to length 27. Her e it should be understood that only one set of vectors, 21 or 22, will b e present in cell 10 but the two different states are illustrated simul taneously in FIG. 1 for convenience. Layers 11 and 13 are coupled by a f erromagnetic coupling which allows vectors 21 and 22 to align in the sam e direction in the absence of an external magnetic field. This coupling is a function of the material and the thickness of layer 12.

Additionally width 26 is formed to be smaller than the width of the magn etic domain walls or transition width within layers 11 and 13. Consequen tly, vectors 21 and 22 cannot be parallel to width 26. Typically, widt hs of less than 1.0 to 1.2 microns result in such a constraint. In this example, width 26 is less than one micron and is as small as can be mad e by manufacturing technology, and length 27 is approximately five times width 26. Also in this example, thickness 23 is approximately three t o six nanometers and thickness 24 is approximately four to ten nanometer s. As will be seen hereinafter, the difference in thickness 23 and 24 a ffects the switching points of layers 11 and 13. Vectors 21 and 22 illu strate two different states of magnetization vectors within cell 10. On e state is referred to as a logic "0" and the other state is a logic "1" . For each state vectors in both layers 11 and 13 point in a first dire ction, and for the other state vectors in both layers 11 and 13 point in the opposite or second direction.

To write or change the state of cell 10, a total magnetic field is appli ed that is sufficient to completely switch the direction of the magnetic

vectors of both layers 11 and 13 from along one direction of easy 27 to along the opposite direction of length 27, that is, to switch from the state represented by vectors 21 to the state represented by vectors 22 or vice versa. To provide the total magnetic field, a transverse conductor or word line 16 is formed on the surface of a dielectric 14 overlying memory cell 10 and a second conductor (not shown) is connected to opposite ends of cell 10 in individual rows to form a sense line. A combination of the sense line and word line 16 are also used to read, or sense, the state stored in cell 10. It should be noted that in some cases, an additional digit line (not shown) which is perpendicular to word line 16 is required to ensure that the value of the total magnetic field is sufficient to cause the magnetic vectors to either rotate or to switch. The value of the total magnetic field is a summation of the magnetic fields resulting from the sense, word, and digit line currents.

FIG. 2 is a graph 31 illustrating the resistance or voltage output of cell 10 (FIG. 1) verses the applied magnetic field or total magnetic field. The abscissa indicates magnetic field direction and strength, that is, the strength either supports or opposes the magnetic vectors of cell 10. The ordinate represents the voltage output of cell 10. A curve 32 indicates the magnetoresistance characteristic, via the output voltage, for various magnetic field intensities for one direction of magnetization vectors (for example vectors 21). A curve 33 indicates the magnetoresistance characteristic, via the output voltage, for the same magnetic field intensities for the opposite direction of magnetization vectors (for example vectors 22). To the right of zero, curves 32 and 33 indicate the output voltage for magnetic fields that support the vectors of curve 32 and oppose the vectors of curve 33, and magnetic fields to the left of zero support the vectors of curve 33 and oppose the vectors of curve 32. Typically, curves 32 and 33 cross the voltage axis at the same point

and have the same minimum values. For the sake of explanation, curve 3
3 is shifted vertically a slight amount to show the differences between
the curves.

At zero applied field, the voltage output of cell 10 is approximately th
e same regardless of the magnetization vector direction. As the field i
ncreases from zero to H1, curve 33 shows the voltage output of cell 10 h
aving vectors that are opposed by the total magnetic field, and curve 32
shows the voltage of cell 10 having vectors that are supported by the m
agnetic field. At magnetic field intensity of H1, the vectors of the la
yer 11 begin to rotate and increase the output voltage. As the total ma
gnetic field intensity increases between H1 and H3, the magnetic vectors
of layer 11 continue to rotate and snap to the other direction near a f
ield intensity of H3. Near H4, the vectors of thicker layer 13 snap to
the opposite direction and the resistance decreases for values of H4 and
above. Similarly, the output voltage for an opposite direction total m
agnetic field is shown between zero and H5 to H8.

The resistance is normally determined by sensing a voltage output of cel
l 10. The voltage output is the voltage drop across the length of cell
10 with a constant current applied along the length of cell 10 and while
a magnetic field is applied. One method of determining the state of ce
ll 10 is to apply a total magnetic field that is higher than the switchi
ng threshold for layer 11 (i.e. H3) but not as high as the switching thr
eshold for layer 13 (i.e. H4). When the total magnetic field is in a di
rection that supports the magnetic vectors, that is, in the same direct
on along length 27 as the magnetization vectors, the magnetic vectors do
not substantially rotate so the resistance of cell 10 does not substant
ially change. Correspondingly, the output voltage also does not substan
tially change.

However, when the total magnetic field opposes the vectors, the magnetic

vectors rotate. As the field increases the vectors of layer 11 begin to rotate toward the opposite end of layer 11 (the vectors of layer 13 may rotate slightly). As the field increases further, the vectors of layer 11 continue to rotate and the resistance increases until the vectors snap to the opposite direction. For further increases, the resistance remains substantially constant until the vectors of layer 13 also snap, which produces a change in stored information. Thereafter, the resistance decreases as the field increases.

Because cell 10 operates on the premise that the value of the total magnetic field is a summation of the magnetic fields resulting from the sense, word, and digit line currents, it can be seen that stray magnetic fields combined with the total magnetic field can produce substantial errors in either of the reading or writing operations, as well as effecting cell 10 during normal storage. For example, during reading operations, when a total magnetic field is higher than the switching threshold of layer 11 but not sufficient to switch the magnetic vectors of layer 13, a stray magnetic field could easily supply a sufficient total magnetic field to surpass Hs and actually switch the information in the cell. Further, because many of the memory cells are very small and packed very closely together, especially in large arrays, a relatively small amount of stray magnetic field can have a substantial effect thereon.

To alleviate the stray magnetic field problem, a passivation layer 15 is formed at least partially surrounding memory cell 10. In a preferred embodiment, layer 15 is formed of a layer of non-conductive high permeability material, such as ferrite material. Some ferrite materials that are suitable for the described purpose are at least one of: Mn-Zn-Ferrite, Ni-Zn-Ferrite, MnFeO, CuFeO, FeO, and NiFeO. Because layer 15 is non-conductive, it can be deposited directly on the surface of cell 10 or a thin layer 17 of dielectric material may be used between cell 10 and layer

r 16, if layer 18 is sufficiently conductive to affect the operation. B
ecause layer 18 is formed of a high permeability material any stray magn
etic fields are shielded from cell 10. Further, any magnetic field prod
uced by current being applied to word line 16 is focused or directed ont
o cell 10 by layer 18 so that a smaller amount of current can be applied
to word line 16 to achieve the same amount of total magnetic field requ
ired for reading and/or writing.

Thus, layer 18 performs the dual function of shielding cell 10 against s
tray magnetic fields and focusing internally generated magnetic fields w
ithin cell 10. In the event that only the shielding function is desired
, layer 18 can be formed of a typical passivation material (any conventio
nal dielectric material which provides a good barrier to external moistur
e, etc.) with a quantity of high permeability material intermixed. Gene
rally the high permeability material can be powdered and mixed with the
passivation material in a liquid or semi-liquid form and then applied to
the cell or array or molded around the cell. Also, the high permeabili
ty material can be sputtered or spun-on along with the passivation mater
ial. In yet another application technique, powders of the ferrite mater
ials can be spray coated onto the passivation layer, or on the back of t
he substrate, or onto the package as a very low cost deposition method.

Turning now to FIG. 2, a simplified and enlarged cross-sectional view of
an array 50 of cells, similar to cell 10, is illustrated. Only a portio
n of array 50 is illustrated for convenience, including cells 51 and 52
. Typically, a plurality of cells (e.g. 51 and 52) similar to cell 10 a
re formed on a common substrate 55 with a space between each individual
cell 51, 52, etc. A conductor 56 is then applied to interconnect cells
51, 52, etc. in individual rows (sense lines). A plurality of transvers
e conductors or word lines 57 are associated in overlying relationship o
ne each with each column of the memory cells.

A passivation layer 60 is formed over the entire array to completely passivate the entire array and any integrated circuits (illustrated in block form at 61) associated with the array. Passivation layer 60, in a preferred embodiment is formed of a layer of ferrite materials which are sputtered or spun-on using any of the well known techniques. Once the entire passivation layer 60 is formed, openings 65 are formed through passivation layer 60 to allow connections to bonding pads and the like. In this preferred embodiment, passivation layer 60 not only passivates and shields the array but focuses or directs internally generated magnetic fields (e.g. those generated by current in word lines 57) onto the associated cells. As previously described, if only the functions of shielding and passivation are desired, passivation layer 60 is formed of a passivating material with powdered or small particles of a high magnetic permeability material intermixed therein.

Thus, a new and improved non-volatile magneto-resistive memory with stray magnetic shielding has been disclosed. The stray magnetic shielding does not add substantially to the cost of the memory because it is simple and easy to apply, generally being incorporated into a procedure which is already in place as, for example, the standard passivation technique. In a preferred embodiment, the stray magnetic shielding for the new and improved non-volatile magnetic-resistive memory also focuses the internally generated magnetic fields of the memory. The focusing of the magnetic fields, along with elimination of stray magnetic fields allows the internally generated magnetic fields to be substantially reduced, which reduces the amount of power required to operate the memory. Further, the focusing reduces the power consumption of the cell, reduces the metal current density and improves the associated metal reliability. The focusing also reduces the size of drive transistors to increase cell real estate efficiency.

While we have shown and described specific embodiments of the present invention, further modifications and improvements will occur to those skilled in the art. We desire it to be understood, therefore, that this invention is not limited to the particular forms shown and we intend in the appended claims to cover all modifications that do not depart from the spirit and scope of this invention.

What is claimed is:

1. Stray magnetic shielding for a non-volatile magneto-resistive memory comprising:

a non-volatile magneto-resistive memory (10, 50) positioned on a substrate and defining an upper surface; and

a passivation layer (18, 60) at least partially surrounding the non-volatile magneto-resistive memory (10, 50), the passivation layer (18, 60) including ferrite materials for shielding the non-volatile magneto-resistive memory (10, 50) from stray magnetic fields.

2. Stray magnetic shielding for a non-volatile magneto-resistive memory comprising:

a non-volatile magneto-resistive memory (10) positioned on a substrate and defining an upper surface, the non-volatile magneto-resistive memory (10) including at least first and second layers (11, 13) of magneto-resistive material separated by a layer (12) of non-magnetic material;

a layer (18) of high permeability, non-conductive magnetic material positioned adjacent the upper surface of the non-volatile magneto-resistive memory (10) so as to focus internally generated magnetic fields on at least one of the first and second layers (11, 13) of magneto-resis

tive material and shield the non-volatile magneto-resistive memory (10) from stray magnetic fields; and

a passivation layer (18) at least partially surrounding the layer of high permeability, non-conductive magnetic material (16) and the non-volatile magneto-resistive memory (10).

3. Stray magnetic shielding for a non-volatile magneto-resistive memory comprising:

a non-volatile magneto-resistive memory (50) positioned on a semiconductor substrate (55), the non volatile magneto-resistive memory (50) including an array of individual cells (51, 52) with each cell including at least first and second layers of magneto-resistive material separated by a layer of non-magnetic material, the non volatile magneto-resistive memory (50) further including integrated circuitry (61) addressing and controlling the individual cells (51, 52) with input/output terminals; and

a layer of high permeability, non-conductive magnetic material (60) coating at least an upper surface of the non volatile magneto-resistive memory (50) so as to focus internally generated magnetic fields on at least one of the first and second layers of magneto resistive material in each of the individual cells (51, 52) and shield the non-volatile magneto-resistive memory from stray magnetic fields.

4. A method of shielding a non-volatile magneto-resistive memory from stray magnetic fields comprising the steps of:

providing a non-volatile magneto-resistive memory positioned on a substrate and defining an upper surface; and

passivating and shielding the non-volatile magneto-resistive memory from stray magnetic fields by at least partially surrounding the non

-volatile magneto-resistive memory with a layer of passivation material including ferrite materials.

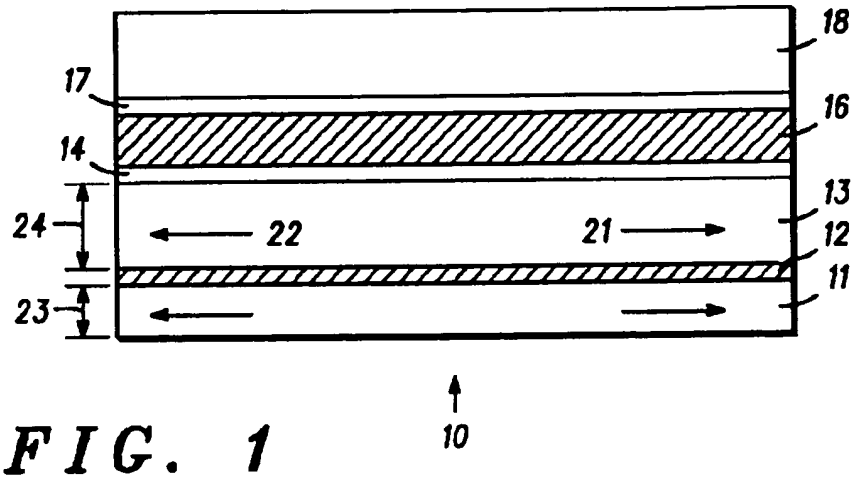
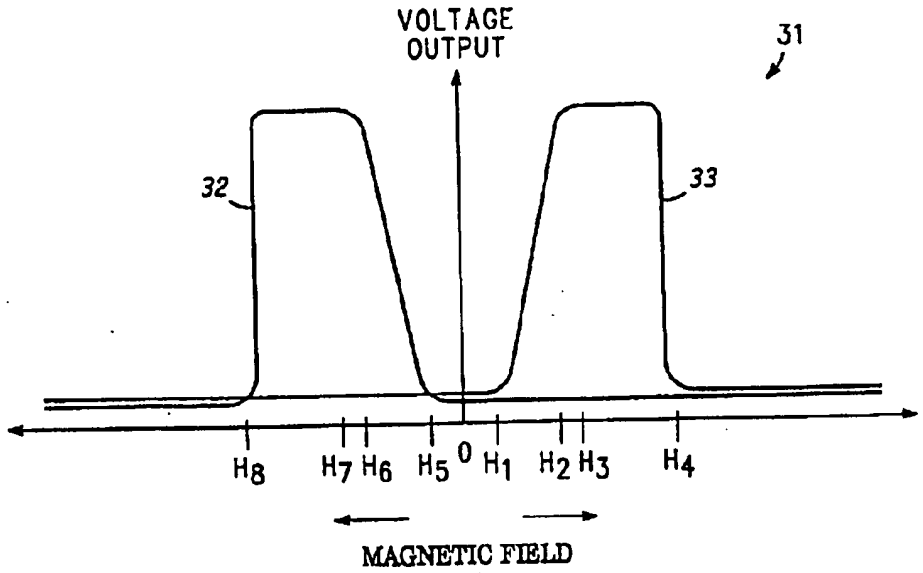

18
17
16
14
13
24
22
21
12
11
23
10

FIG. 1

FIG. 2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H7
H6
H5
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H1
H2
H3
H4
MAGNETIC FIELD

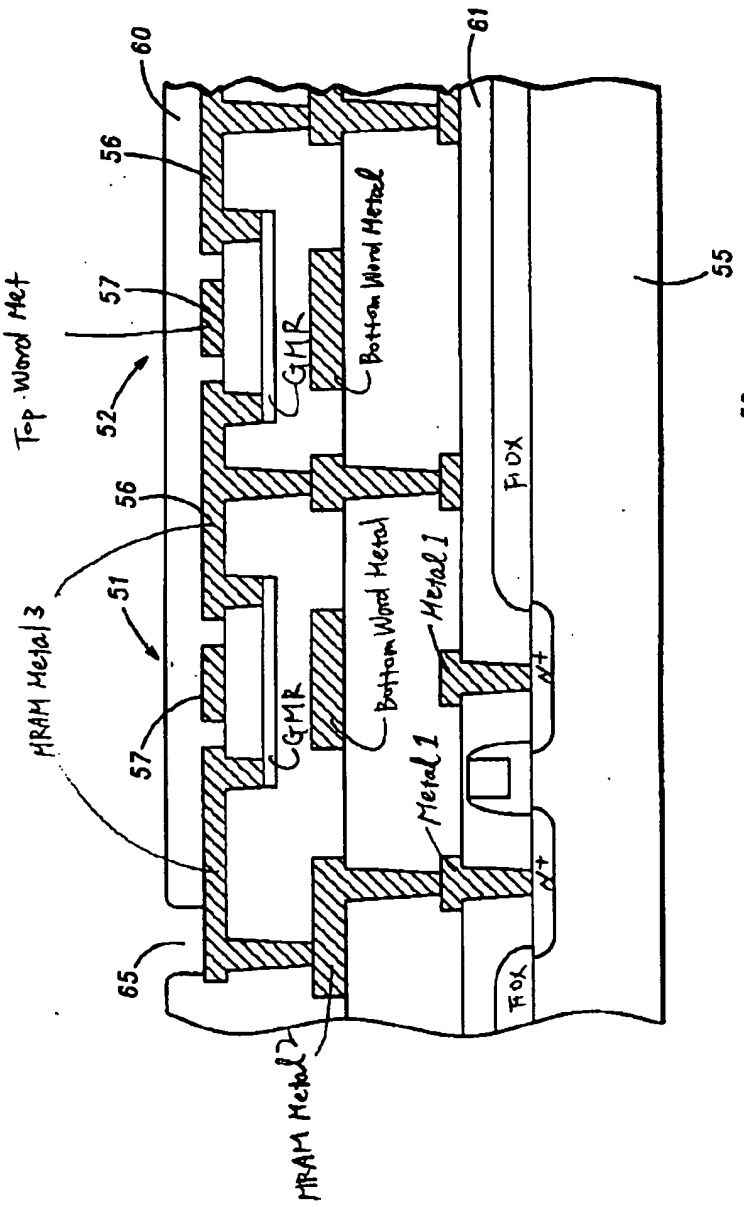
60
61
56
57
52
Top Word Met
GMR
Bottom Word Metal
55
50
56
51
MRAM Metal 3
57
GMR
Bottom Word Metal
Metal 1
FOX
N+
Metal 1
N+
65
FOX
MRAM Metal 2

FIG. 3

Abstract of the Disclosure

A non-volatile magneto-resistive memory (10) positioned on a semiconductor substrate is shielded from stray magnetic fields by a passivation layer (18) partially or completely surrounding the non-volatile magneto-resistive memory (10). The passivation layer (18) includes non-conductive ferrite materials, such as Mn-Zn-Ferrite, Ni-Zn-Ferrite, MnFeO, CuFeO, FeO, or NiFeO, for shielding the non-volatile magneto-resistive memory (10) from stray magnetic fields. The non-conductive ferrite materials may also be in the form of a layer (18) which focuses internally generated magnetic fields on the non-volatile magneto-resistive memory (10) to reduce power requirements.